performing an approximately vertical halo implant through the void to a depth of approximately 40 nm to approximately 100 nm, thereby forming a halo around the gate in the channel region; and

completing the MOSFET.

REMARKS

Applicant has amended the claims to clarify that the method of the present invention is applicable to manufacture of chips having a deep submicron channel of approximately 50 nanometers (nm) or less. Applicant believes the amended claims clearly distinguish from the prior art for reasons discussed below.

In paragraphs 1-3 of the Office Action, the Examiner rejected under 35 U.S.C. 103 claims 1-6 and 8-11 as being made obvious by Pan, U.S. patent 5,595,919 in view of Wu, U.S. patent 6,190,977. The Examiner asserts that it would be obvious to combine two steps from the method of Wu with the method of Pan to arrive at the present invention. Applicant respectfully traverses the Examiner's rejection.

Pan recognizes the need to engineer away the short channel effect, but teaches that the key to his method is the deposition of a thick oxide layer 26 to serve as a mask for subsequent implantation steps (col 3, lines 26-33). Pan does not define a dimension for a "short channel", which is presumably in the micron range. Pan teaches that halos have disadvantages (col 1, lines 31-35), then proceeds to teach a halo having an opposite dosage than the lightly doped junction regions (col 2, lines 4-6), creating the presumption that this is the means to overcome the disadvantages of halos. Pan then further teaches removal of the nitride spacer, followed by two ion implantation steps: one implantation of ions selected from a first group for the source/drain junctions (LDD regions) and one halo implantation over a range of angles from vertical to 40°, with the halo implantation having ions selected from a second group of ions different than the first group (col 3, lines 34-55). Pan therefore teaches that it is necessary to use a halo chosen to counter (n versus p ions) the S/D junction implant (col 3, lines 48-51) to overcome the disadvantages caused by the use of halos. Pan neither suggests nor teaches the use of halos

of similar implanted ions to engineer sub-micron short channel effects, and effectively teaches away from their use unless used to counter the LDD junctions.

As previously noted by the Applicant, Wu recognizes the need to address short channel effects, stating "With the present semiconductor manufacturing technology, the processes with generally a quarter micrometer in size is widely utilized. For making the next generation devices, the technologies focusing mainly on one-tenth micrometer and even nanometer feature sizes are highly required."(col 1, lines 48-53) Wu then teaches that the short channel effect, of gates having channels in the range down to 250 nm, is suppressed by using a shallow S/D junction and S/D regions elevated above the substrate. Wu further teaches that "The unwanted effects accompanying with the narrowed channel region of the small devices are eliminated by the extended ultra shallow junction."(col 6, lines 48-50). Further, Wu specifically teaches the retention of the nitride spacer, thus teaching away from the method of Pan (col 5, lines 62-65). Thus, Applicant respectfully asserts that Wu teaches that nanometer scale short channel effects are eliminated solely by the raised source/drain regions with shallow junctions, without the need or desirability of removing the nitride spacer or forming an ion halo in the channel region. Applicant respectfully asserts therefore that Wu teaches away from Pan and it would not be obvious to combine portions of each method to arrive at the claimed invention.

Nowhere, as best Applicant can determine, does Wu teach or suggest that a halo implantation in combination with raised source/drain regions would be desirable, beneficial or necessary to improve the short channel effect performance of a MOSFET having channel dimensions in the deep submicron range up to 50 nm. Applicant respectfully asserts that this is significant, as Wu, coming three years after Pan, better represents the more current state of the art at that time. In fact, the statement by Wu that short channel effects "are eliminated" by his method would dissuade a practitioner from making changes to Wu's method by adding a halo formation step, thus effectively teaching away from Pan, especially since Pan teaches that halos have disadvantages and that implanted halo ions should oppose the junction implant ions. Applicant respectfully asserts that in the rapidly evolving computer chip-making art, Wu better represents the later state of the art and thus, the absence of any recognition of the usefulness of halo implantation would be significant to a practitioner, and would appear to such practitioner to teach away

from the use of halos, given Pan's warning that halos have disadvantages. Applicant therefore respectfully asserts that Wu would not motivate a practitioner to combine the method of Wu with some of the steps of the method of Pan to arrive at the Applicant's method.

Applicant has discovered and therefore teaches and claims that a single halo of ions implanted vertically around a gate in the channel, in combination with raised source/drain regions, improves the performance of a gate having a deep submicron channel with a dimension up to 50 nm, by improved suppression of the short channel effect. Applicant claims:

A method of making a MOSFET, comprising:
providing a substrate having a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm length;
performing a source/drain extension implant;
forming a spacer on the gate;
performing epitaxy to form raised source/drain regions;
forming a silicide on the gate and source/drain regions;
removing the spacer, thereby forming a void region between the source/drain regions and the gate;
performing a halo implant through the void, thereby forming a halo around the gate in the channel region; and
completing the MOSFET.

Applicant respectfully notes that the removal of the spacer inherently forms a void region, or gap, until such a time as something is placed into the space left by the removed spacer. Thus, no new matter is introduced by the term "void" to refer to the region formerly occupied by the spacer. Applicant respectfully asserts that the cited art, neither individually nor in combination, suggests, teaches or motivates a practitioner to arrive at the presently claimed invention which is directed at engineering of the short channel effect of gates defining channels up to 50 nm. Applicant has recognized and claims a method of making microcircuits having superior channel effects by forming a halo of ions in the channel region when taken in conjunction with raised source/drain regions, a combination neither suggested nor taught by Wu, nor suggested by Pan in view of Wu.

CONCLUSION

Claims 1, 5 and 10 are herein amended to better encompass the full scope and breadth of the present invention, notwithstanding the Applicant's belief that the claims would have been allowable as originally filed. The above amendments are made purely to clarify the invention. Applicant respectfully submits that the presently claimed invention is patentably distinct over the cited references, and Applicant therefore believes that the claims, as amended, now are non-obvious in view of Pan and Wu as required by 35 U.S.C. 103. Therefore Applicant believes the present invention as now claimed is patentable. In view of the foregoing amendment and remarks, favorable consideration by the Examiner, entry of the above amendment, withdrawal of the present rejections, allowance of the pending claims, and passage of the present application to issuance are accordingly solicited. The Examiner is cordially invited to telephone the undersigned for any reason which would advance the pending claims toward allowance.

Respectfully submitted,

Victor Flores

Victor Flores
Reg. No. 29,638

VF/rm
Date: 10/31/02
LARIVIERE, GRUBMAN & PAYNE, LLP
Post Office Box 3140
Monterey, CA 93942
(831) 649-8800

MARKED-UP VERSION OF CLAIMS

1. (AMENDED) A method of making a MOSFET, comprising:

providing a substrate having a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm length;

performing a source/drain extension implant;

forming a spacer on the gate;

performing epitaxy to form raised source/drain regions;

forming a silicide on the gate and source/drain regions;

removing the spacer, thereby forming a void region between the source/drain regions and the gate;

performing a halo implant through the void, thereby forming a halo around the gate in the channel region; and

completing the MOSFET.

5. (AMENDED) A method of making a MOSFET, comprising:

providing a substrate having a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm length;

performing a vertical source/drain extension ion implant to a depth of approximately 10 nm to approximately 30 nm;

forming a spacer on the gate;

forming raised source/drain regions;

forming a silicide on the gate and source/drain regions;

removing the spacer, thereby forming a void region through the silicide between the source/drain regions and the gate;

performing a halo implant through the void, thereby forming a halo around the gate in the channel region; and

completing the MOSFET.

10. (AMENDED) A method of making a MOSFET, comprising:

providing a substrate having a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm;

performing an approximately vertical source/drain extension implant to a depth of approximately 10 nm to approximately 30 nm;

forming a nitride spacer on the gate;

performing epitaxy to form raised source/drain regions;

forming a silicide on the gate and source/drain regions;

removing the spacer, thereby forming a void region through the silicide between the source/drain regions and the gate;

performing an approximately vertical halo implant through the void to a depth of approximately 40 nm to approximately 100 nm, thereby forming a halo around the gate in the channel region; and

completing the MOSFET.